REMARKS

To expedite prosecution, claims 5, 6, 13, 14, and 16 have been canceled; claims 1, 7, 9, 11, 15, and 17 have been amended; claims 23-25 have been added. Thus, claims 1-4, 7-12, 15, and 17-25 are currently pending in the case. Further examination and reconsideration of the presently claimed application is respectfully requested.

Section 103 Rejections

Claims 1-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,093,631 to Jaso et al. (hereinafter "Jaso") in view of pages 1-6 of Applicant's Specification and Figs. 1-4 of Applicant's Drawings (hereinafter "Applicant's Background Disclosure"). To expedite prosecution, claims 5, 6, 13, 14 and 16 have been canceled, thereby rendering their rejections moot. To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond,* 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below. Accordingly, removal of the § 103(a) rejection of claims 1-22 is respectfully requested.

None of the cited art teaches or suggests polishing a conductive material to form dummy conductors between a relatively wide interconnect feature and a series relatively narrow interconnect features by applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material. Amended claim 1 recites, in part:

> A method, comprising: etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches; filling said trenches with a conductive material; and polishing said conductive material to form dummy conductors in said dummy trenches, wherein said polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

Amended claim 9 includes a similar limitation. Support for the amendments to claims 1 and 9 may be found, for example, on page 8, lines 14-17 of the Specification, "In an alternate embodiment, a "fixed-abrasive" technique is used to polish the conductive material. The fixed-abrasive technique involves

placing a liquid which is substantially free of particulate matter between the surface of the conductive material and an abrasive polishing surface of a polishing pad."

Neither Jaso nor the Applicant's Background Disclosure teaches or suggests polishing a topography using fixed abrasive techniques to form dummy structures therein. More specifically, neither Jaso nor the Applicant's Background Disclosure teaches or suggests polishing a conductive material to form dummy conductors between a relatively wide interconnect feature and a series relatively narrow interconnect features by applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material as recited in the presently claimed case. On the contrary, Jaso and the Applicant's Background Disclosure restrict their discussions of polishing to techniques which include applying an abrasive chemical slurry between a polishing pad and a topography. There is no discussion within Jaso or the Applicant's Background Disclosure of using a polishing pad with abrasive particles embedded therein or a polishing solution which is substantially absent of particulate matter. In fact, Jaso specifically teaches that, "... the chemical-mechanical planarization (CMP) process involves pressing a semiconductor wafer against a moving polishing surface that is wetted with a chemically reactive, abrasive slurry ... The polishing surfaces typically are a planar pad made of a relatively soft, porous material ..." (Emphasis added. Jaso, column 1, lines 40-46). Since none of the cited art teaches or suggests the limitations of claims 1 and 9, none of the cited can provide any motivation to teach the limitations of claims 1 and 9. As such, claims 1 and 9 are asserted to be patentably distinct over the cited art.

None of the cited art teaches or suggests a semiconductor topography with a plurality of laterally spaced dummy trenches between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches. Amended claim 17 recites, in part:

> A substantially planar semiconductor topography, comprising: a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches ...

Support for the amendment to claim 17 may be found, for example, on page 13, lines 17-19, "... dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have sub-micron widths, and the wide trench 54 is preferably greater than 50 microns in width."

As noted in the Office Action and in a response to a previous Office Action mailed July 3, 2002, Jaso does not disclose a topography with dummy trenches interposed between a relatively wide trench and a series of relatively narrow trenches. As such, Jaso cannot teach or suggest a topography with a dummy trench having a lateral dimension which is less than a lateral dimension of an adjacent relatively wide trench and greater than a lateral dimension of an adjacent series of relatively narrow trenches as recited in claim 17. Moreover, the Applicant's Background Disclosure does not even disclose a topography with a dummy trench, much less a topography with a dummy trench having a lateral dimension which is smaller and larger than the lateral dimensions of trenches arranged adjacent to the dummy trench. Consequently, the Applicant's Background Disclosure can neither teach a topography with the limitations of claim 17 nor be combined with Jaso to teach a topography with such limitations. Since none of the cited art teaches or suggests the limitations of claim 17, none of the cited can provide any motivation to teach the limitations of claim 17. As such, claim 17 is asserted to be patentably distinct over the cited art.

Patentability of Added Claims

The present Amendment adds claims 23-25. Claims 23-25 are dependent from base claim 17 and, therefore, are patentably distinct over the cited art for at least the same reasons as that claim. Accordingly, allowance of added claims 23-25 is respectfully requested.

NOTICE OF CHANGE OF ATTORNEY DOCKET NUMBER

The Commissioner is requested to change the attorney docket number for the above-identified patent application as set forth below.

Old Number:	5298-02501
New Number:	5298-02502

CONCLUSION

This response constitutes a complete response to all issues raised in the final Office Action mailed December 17, 2002. In view of the remarks traversing rejections presented therein, Applicants assert that pending claims 1-4, 7-12, 15, and 17-25 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-02502.

Respectfully submitted,

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ATTACHMENT A
"Marked-Up" Amendments

IN THE CLAIMS

Please cancel claims 5, 6, 13, 14, and 16. Please amend claims 1, 7, 9, 11, 15, and 17 as follows. Also following is list of all remaining pending claims.

1. (Thrice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material; and

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said series of relatively narrow trenches and said relatively wide trench, wherein said [dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit] polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

2. The method of claim 1, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

3. The method of claim 1, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said series of relatively narrow trenches and said relatively wide trench.

4. The method of claim 1, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

5. (Canceled)

6. (Canceled)

7. (Amended) The method of claim [5] 1, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

8. The method of claim 1, wherein said polishing comprises placing a CMP slurry onto a polishing pad surface, and contacting said polishing pad surface with an upper surface of said conductive material while rotating said polishing pad surface relative to said upper surface.

9. (Twice Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said [dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit] polishing comprises applying a liquid substantially free of particulate matter between an abrasive polishing surface and the conductive material.

10. The method of claim 9, wherein said conductive material comprises a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

11. (Twice Amended) The method of claim 9, wherein said polishing said conductive material is performed at a substantially uniform polish rate above said dummy trenches and said [said] trench and said series of trenches.

12. The method of claim 9, wherein said polishing results in dummy dielectric protrusions between adjacent pairs of said dummy trenches, said dummy dielectric protrusions having first upper surfaces substantially coplanar with second upper surfaces of said dummy conductors.

13. (Canceled)

14. (Canceled)

15. (Amended) The method of claim [13] 9, wherein said abrasive polishing surface comprises particles at least partially fixed into a polymer-based matrix, and wherein said particles comprise a material selected from the group consisting of cerium oxide, cerium dioxide, aluminum oxide, silicon dioxide, titanium oxide, chromium oxide, and zirconium oxide.

16. (Canceled)

17. (Thrice Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches, wherein a lateral dimension of at least one of the dummy trenches is less than a lateral dimension of the wide trench and greater than a lateral dimension of at least one of the series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said series of relatively narrow trenches and said relatively wide trench, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

18. The substantially planar semiconductor topography of claim 17, further comprising dummy dielectric protrusions between adjacent pairs of said laterally spaced dummy trenches, said dummy dielectric protrusions having dummy dielectric upper surfaces substantially coplanar with said dummy conductor upper surfaces.

19. The substantially planar semiconductor topography of claim 17, wherein said dummy conductors comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

20. The substantially planar semiconductor topography of claim 17, wherein said interconnect comprise a metal selected from the group consisting of aluminum, copper, tungsten, molybdenum, tantalum, titanium, and alloys thereof.

21. The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.

Please add the following claims:

23. (Added) The substantially planar semiconductor topography of claim 17, wherein lateral dimensions of the dummy trenches are between approximately 1 micron and approximately 5 microns.

24. (Added) The substantially planar semiconductor topography of claim 17, wherein the lateral dimension of the wide trench is greater than approximately 50 microns.

25. (Added) The substantially planar semiconductor topography of claim 17, wherein the relatively narrow trenches comprise sub-micron lateral dimensions.